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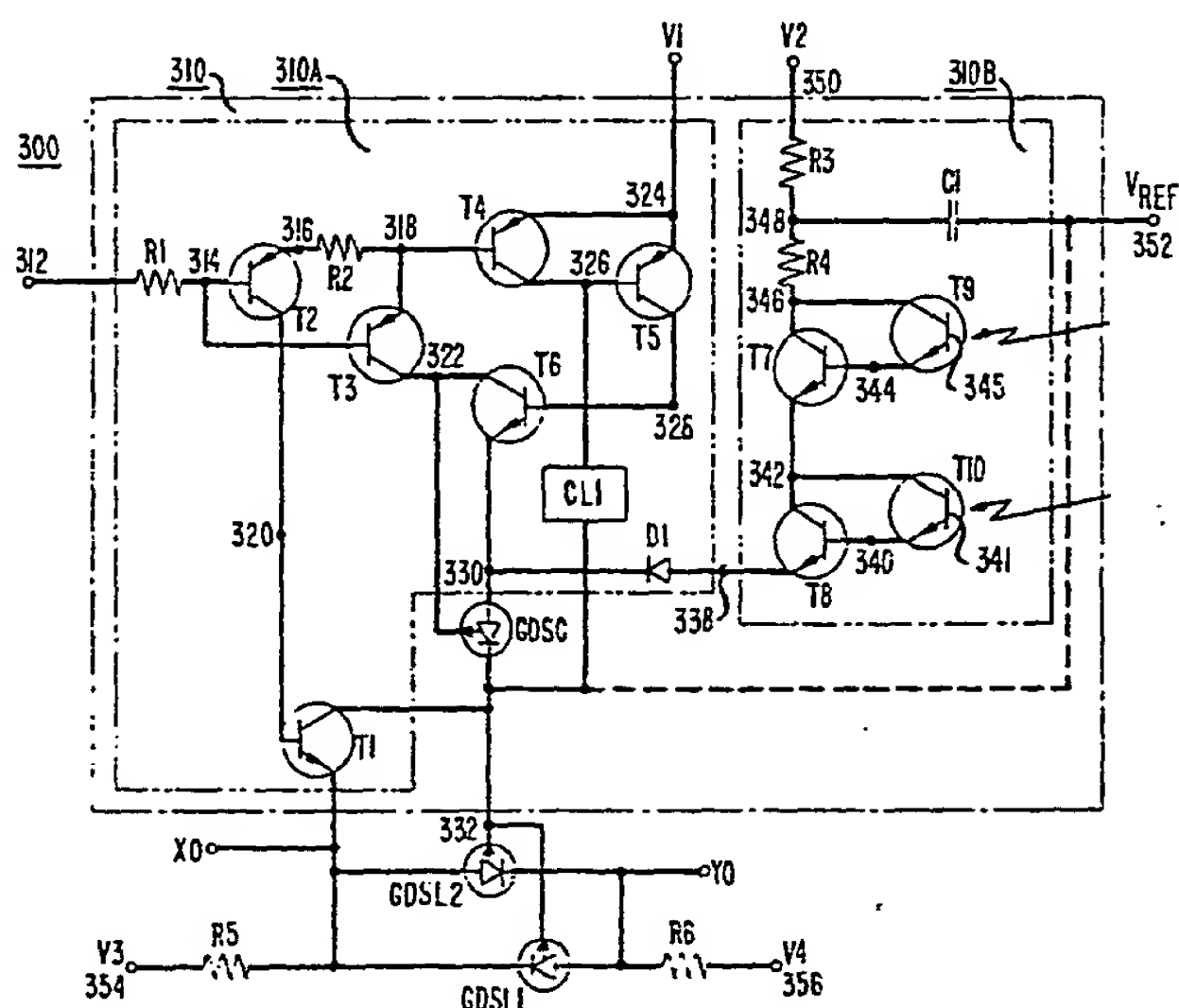
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(54) Title: CONTROL CIRCUITRY USING A PULL-DOWN TRANSISTOR FOR HIGH VOLTAGE SOLID-STATE SWITCHES

## (57) Abstract

To switch a first gated diode switch (e.g. GDSC1) to the „OFF“ state requires a voltage applied to the gate which is more positive than that of the anode or cathode and the sourcing of current into the gate which is of the same order of magnitude as flows between the anode and cathode. Control circuitry, which uses a second (e.g. GDSC) coupled by the cathode to the gate of the first GDS, is used to control the state of the first GDS. The state of the second GDS is controlled by a branch circuit (e.g. 510A) having a relatively modest current handling capability. An n-p-n junction transistor (e.g. T1) has the emitter and collector coupled to the cathode and gate, respectively, of the first GDS, and has the base coupled through a p-n-p transistor (e.g. T2) to the input terminal of the control circuitry. The n-p-n transistor facilitates a quick turn-on of the first GDS by rapidly bringing the potentials of the gate and cathode of the first GDS to levels which are close together.



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CONTROL CIRCUITRY USING A PULL-DOWN  
TRANSISTOR FOR HIGH VOLTAGE SOLID-STATE SWITCHES

Background of the Invention

This invention relates to control circuitry for  
5 controlling the state of solid-state switches and, in  
particular, to control circuitry for controlling the state  
of solid-state switches which have high voltage and  
relatively high current capabilities.

High voltage and relatively high current  
10 capability solid-state switches, such as one described in  
an article entitled "A Field Terminated Diode" by  
Douglas E. Houston et al, published in IEEE Transactions on  
Electron Devices, Vol. ED-23, No. 8, August 1976, and that  
described in "A 500V Monolithic Bidirectional 2 x 2 Cross  
15 Point Array," by P. Shackle et al., IEEE International  
Solid State Circuits Conference, Feb., 1980, p. 170-171,  
have an ON (conducting) state and an OFF (blocking) state.  
These switches are capable of blocking relatively large  
potential differences in the OFF state. Each of these  
20 switches has two output terminals which are generally  
denoted as the anode and cathode, a control terminal which  
is generally denoted as the gate, and a semiconductor body  
whose bulk separates the anode, cathode, and gate regions.  
The parameters of the various portions of the semiconductor  
25 are such that with the potential of the anode region being  
greater than that of the cathode region and the potential  
of the gate region being insufficient to cause the  
potential of a vertical cross-sectional portion of the bulk  
of the semiconductor body between the anode and cathode to  
30 be greater in potential than the anode or cathode regions  
there is facilitated a substantial current flow between the  
anode and cathode regions via the bulk. With the potential  
of the gate region being sufficiently more positive than  
that of the anode and cathode regions to cause a vertical  
35 cross-sectional portion of the bulk of the semiconductor



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body between the anode and cathode regions to be more positive in potential than the anode and cathode regions there is facilitated an interrupting or inhibiting of current flow between the anode and cathode regions. The  
5 magnitude of the needed gate potential necessary to turn off these switches is a function of the geometry and doping levels of the semiconductor regions of each switch and of the anode and cathode potentials.

Control circuitry used to apply a blocking  
10 voltage to the gate terminal of each of these switches must be able to sustain a more positive voltage than is at the anode and cathode terminals and must be able to supply current which is generally of the same magnitude as flows through the anode and cathode of each switch.

15 Control circuitry is known which itself uses a high voltage and current switch of the type described hereinabove to control the state of a similar switch. If a control circuit should fail to break (interrupt) current flow through an ON switch connected thereto, it is  
20 necessary to electrically disconnect the control circuitry from one of the supply potential sources. The control circuitry is then reset and reconnected to the potential source. It is then activated again so as to break conduction through the ON switch.

25 Usually a conventional high voltage and high current capability switch is used between the high voltage source and the control circuitry. This switch can be an optically activated switch. Generally it is a relatively expensive component and only one is used for a relatively  
30 large number of control circuits. If any of the switches to be controlled fails to turn off, it is necessary to disconnect all the control circuits from the power supply. This may result in all of the switches connected to the control circuitries being switched to the ON state  
35 independent of which state is desired. This is undesirable in some switching applications. The speed of operation and power dissipation of the above-described control circuitry



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may be slower and higher, respectively, than is desired in some switching applications.

It would be desirable to have circuitry capable of controlling high voltage and high current solid-state switches of the type discussed hereinabove which has improved switching time and lower power dissipation than prior art circuitry, and which can maintain some switches connected thereto in the desired state even if one of the switches being controlled fails to break current (assume the OFF state).

#### Summary of the Invention

The present invention is directed to control circuitry for controlling the state of high voltage and relatively high current solid-state switches of the type described hereinabove. This circuitry essentially comprises a control switch (GDSC) which, in a preferred embodiment, is a gated diode switch, a first branch circuit coupled thereto to control the state thereof, and a circuit means which in the preferred embodiment is an n-p-n transistor (T1) whose emitter is coupled to one of the output terminals of a load switch (GDSL1) which is to be controlled and whose collector is coupled to the gate of GDSL1. The base of T1 is coupled to the first branch circuit which, in turn, is coupled to an input terminal of the control circuitry. One output terminal of GDSC, typically, the cathode terminal, is coupled to the gate of GDSL1.

With a low, voltage, or a "0", input signal applied to the input terminal, T1 becomes biased ON and conducts such that the potential of the collector and emitter become fairly close to each other. These are also the gate and cathode or anode terminals of GDSL1. Accordingly, GDSL1 is switched to an "ON" (conducting) state if proper operating potentials are applied to the anode and cathode terminals. The branch circuit causes GDSC to be turned to the OFF state when it is desired that GDSL1 be in the ON state. When it is desired to switch



GDSL1 to the OFF (nonconducting) state the potential of the input terminal is brought to a high, a "1", level. This causes GDSC to be switched to the ON state, and thus couples the potential of a potential source coupled to its anode to the gate of GDSL1. In addition, positive charge flows from the potential source into the gate of GDSL1. There is provided a sufficiently positive potential on the gate of GDSL1 and a sufficient current flow into the gate to switch GDSL1 to the OFF state.

10 The circuit means comprising n-p-n transistor T1 quickly discharges the potential of the gate of GDSL1 to a level at which the ON state can be achieved. This results in GDSL1 being able to rapidly switch to the ON state soon after the input signal is pulsed to the low level.

15 Brief Description of the Drawing

FIG. 1 illustrates a solid-state bidirectional switch;

FIG. 2 illustrates a solid-state structure;

FIG. 3 illustrates control circuitry in accordance with one embodiment of the present invention; and

FIG. 4 illustrates control circuitry in accordance with another embodiment of the present invention.

25 Detailed Description

Referring now to FIG. 1, there is illustrated a semiconductor structure 10 comprising two gated diode switches, GDS1 and GDS2, which are illustrated within dashed line rectangles and are both formed on a common support member 12. Support member 12 is typically a semiconductor wafer or a substrate. Dielectric layers 14 and 14a separate monocrystalline semiconductor bodies 16 and 16a, respectively, from support member 12 and from each other. Support member 12 has a major surface 11 and bodies 16 and 16a each have a portion that is common with surface 11. Although only two gated diode switches are illustrated, a plurality of dielectrically isolated gated



diode switches of the type of GDS1 and/or GDS2 can be formed in a common semiconductor wafer or substrate 12.

GDS1 and GDS2 are illustrated having electrical connections therebetween which facilitate the use thereof as a bidirectional high voltage switch. GDS1 and GDS2 need not be electrically connected and each can function independently of the other.

In one typical embodiment, support member 12 is a semiconductor wafer (substrate) of n or p type conductivity and semiconductor bodies 16 and 16a have bulk portions thereof which are of p- type conductivity. The semiconductor regions contained within semiconductor body 16 are very similar to those contained in body 16a. A localized anode region 18, which is typically of p+ type conductivity, is included in body 16 and has a portion thereof that extends to surface 11. Surrounding anode region 18 is a p type region 42 which also has a portion thereof which extends to surface 11. Surrounding region 42 is a p- type region 43 which also has a portion thereof which extends to surface 11. The conductivity of region 42 is intermediate that of anode region 18 and semiconductor body 16, and the conductivity of region 43 is intermediate that of region 42 and semiconductor body 16. Electrode 28 makes contact to region 18 and is separated from portions of surface 11 other than those over the exposed portion of region 18 by dielectric layer 26. A localized gate region 20 of n+ type conductivity is included in body 16 and has a portion thereof which extends to surface 11 and is separated from region 42 by portions of the bulk of semiconductor body 16. An electrode 30 contacts region 20 at surface 11. Electrode 30 is separated from portions of surface 11 other than those over the exposed portion of region 20 by dielectric layer 26. A localized cathode region 24, which is of n+ type conductivity, is included in body 16 and is separated from region 20 by portions of the bulk of semiconductor body 16. Region 24 is surrounded by a p+ type guard ring 40 which, in turn, is surrounded by a





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p type region 22 which, in turn, is surrounded by a guard ring like p type region 46. Region 46 can extend, as is illustrated by the dashed line, to essentially completely surround region 22, except for the portions thereof common to surface 11. Region 46 is separated from regions 20 and 43 by portions of the bulk of semiconductor body 16. Electrode 32 contacts region 24 and a separate electrode 50 contacts region 40. Both electrodes are separated from portions of surface 11 other than over the respective exposed portion of regions 24 and 40. A layer 48 of n type conductivity exists between the dielectric layer 14 and semiconductor body 16. Layer 48, which is part of a preferred embodiment, is shown in dashed line since it is optional. Gate region 20 also serves as the collector of a lateral n-p-n transistor with cathode region 24 serving as the emitter and regions 46, 22, and 40 serving as the base.

Semiconductor body 16a contains regions which are very similar to those contained within semiconductor body 16 with the exception of the fact that the p+ type guard ring region 40a does not have a separate electrical contact thereto as does guard ring 40.

GDS1 is typically operated as a switch which has a low impedance between anode region 18 and cathode region 24 when in the ON (conducting) state and as a high impedance between said two regions when in the OFF (nonconducting) state. With operating potentials applied to anode region 18 and cathode region 24, the potential applied to gate region 20 determines the state of the switch. Conduction between anode region 18 and cathode region 24 can occur if the potential of the gate region 20 is near or below the potential of the anode region 18, cathode region 24, and region 22. During the ON state holes are injected into body 16 from anode region 18 and electrons are injected into body 16 from cathode region 24. This effectively lowers the resistance of body 16 such that the resistance between anode region 18 and cathode region 24 is relatively low when GDS1 is operating in the





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ON state. This type of operation is denoted as dual carrier injection and the type of structure described therein has been denoted as a gated diode switch (GDS). Guard ring region 40 and regions 22 and 46 help limit the punch-through of a depletion layer formed during operation between gate region 20 and cathode region 24 and help to inhibit the formation of a surface inversion layer between these two regions. In addition, they facilitate gate region 20 and cathode region 24 being relatively closely spaced apart. This facilitates relatively low resistance between anode region 18 and cathode region 22 during the ON state.

Substrate 12 is typically held at the most positive potential level available. Conduction between anode region 18 and cathode region 24 is inhibited or cut off if the potential of gate region 20 is sufficiently more positive than that of anode region 18 and cathode region 24. The amount of excess positive potential needed to inhibit or cut off conduction is a function of the geometry and impurity concentration (doping) levels of GDS1. This positive gate potential causes a portion of body 16 between gate region 20 and the portion of dielectric layer 14 therebelow to be at a potential that is more positive than that of anode region 18, cathode region 24, and region 22. This positive potential barrier inhibits the conduction of holes from anode region 18 to cathode region 24. It essentially pinches off body 16 against dielectric layer 14 in the bulk portion of semiconductor body 16 below gate region 20 and extending down to dielectric layer 14. It also serves to collect electrons emitted at cathode region 24 before they can reach anode region 18. Control circuitry in accordance with the present invention for controlling gated diode switches like GDS1 and/or GDS2 is illustrated and described in FIGS. 3 and 4 herein.

The ON state can be achieved by allowing gate electrode 30 to electrically float in potential, forward-



biasing the anode region 18 with respect to the cathode region 24, and applying a potential to electrode 50 which forward-biases the emitter-base junction comprising base regions 46, 22, and 40 and emitter (cathode) region 24.

- 5 Once GDS1 is on, if electrode 50 is allowed to electrically float in potential, then GDS1 can be maintained in the ON state with the potential of gate region 20 at the same or a more positive level than anode region 18 and cathode region 24, so long as the potential of gate region 20 is  
10 below the level which essentially completely depletes a vertical cross-sectional portion of semiconductor body 16 between anode region 18 and cathode region 24 and from surface 11 to the top of dielectric layer 14 and causes the potential of this cross-sectional portion to be greater  
15 than that of the anode, cathode, and regions 22, 40, 46.

- As has been earlier denoted, region 20, in addition to serving as the gate terminal of the gated diode switch, serves as the collector of a lateral n-p-n transistor with regions 46 and 22 serving as the base and  
20 region 24 serving as the emitter. Region 40, which also serves as part of the base, is typically of p+ type conductivity and, thus, serves as an electrical contact to region 22. Electrode 50 contacts region 40 and thus allows the base of the n-p-n transistor to be controlled. If  
25 electrode 50 is held at a positive potential with respect to electrode 32, then the n-p-n transistor is biased on and the potential between gate region 20 (the collector of the transistor) and cathode region 24 (the emitter of the transistor) is relatively small. Typically this  
30 collector-emitter voltage is on the order of several tenths to several volts. The potential of gate region 20 is thus drawn to a level close to that of the cathode region 24. This effectively reduces the gate potential to a level which is insufficient to cause the GDS to be in the OFF  
35 state with proper operating potentials applied to the anode and cathode regions. The adjusting of the potential applied to electrode 50 to forward-bias the n-p-



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n transistor facilitates GDS1 being relatively rapidly switched to the ON state.

Semiconductor body 16a contains essentially the same regions as semiconductor body 16, except that guard  
5 ring 40a does not have an electrical contact thereto. Thus, no external control of the base potential of the n-p-n transistor which comprises region 20a as the collector, regions 46a, 22a, and 40a as the base, and region 24a as  
10 the cathode is possible. The size of GDS1 is only slightly larger than that of GDS2. The portion of region 40 which is contacted by electrode 50 is somewhat larger than the corresponding region 40a and, accordingly, region 22 is somewhat larger than region 22a.

The electrical connections shown between  
15 electrodes 28 and 32a to a terminal X, electrodes 30 and 30a to a terminal G, and electrodes 32 and 28a to terminal Y, couple GDS1 and GDS2 together so as to form a bidirectional switching element whose equivalent circuit is illustrated in FIG. 3 herein.

20 Referring now to FIG. 2, there is illustrated a structure 10,000 comprising a semiconductor support member 12,000 having a major surface 11,000 and a monocrystalline semiconductor body 16,000 whose bulk is of p type conductivity and is separated from support  
25 member 12,000 by a dielectric layer 14,000. A p+ type conductivity contact region 34,000 and an n+ type conductivity region 35,000 exist within a portion of support member 12,000 and are both coupled to an electrode 36,000 coupled thereto. Electrode 36,000 is  
30 electrically isolated from all portions of surface 11,000, except where it contacts regions 34,000 and 35,000, by a dielectric layer 26,000.

Support member 12,000 could, and usually does, include at least one other dielectrically isolated  
35 semiconductor bodies (not illustrated) like semiconductor body 16 of FIG. 1. Localized first and second separated p+ type conductivity regions 18,000 and 24,000 are included



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in body 16,000 with each having a portion that forms a part of surface 11,000. A localized region 42,000 of p type conductivity encircles region 18,000. A localized region 22,000 of p type conductivity encircles region 22,000 and is itself encircled by a region 46,000 which is of p- type conductivity. Semiconductor regions of relatively low resistivity are denoted as of p+ or n+ type conductivity. Those of relatively high resistivity are denoted as of p- or n- type conductivity. Those of intermediate resistivity are denoted as p or n type conductivity. A localized n+ type conductivity region 20,000 is included in body 16,000 and is located in between regions 18,000 and 24,000. An electrode 28,000 is coupled to regions 18,000 and 20,000. A separate electrode 32,000 is coupled to region 24,000. Electrodes 28,000 and 32,000 are separated from surface 11 except where they contact the respective regions by dielectric layer 26,000.

Structure 10,000 acts essentially as a pinch resistor with region 20,000 pinching off semiconductor body 16,000 to create a relatively high resistance region between the bottom of region 20,000 and the top of dielectric layer 14,000. Structure 10,000 acts to limit current flow between regions 18,000 and 24,000. Within a first range of potential difference between regions 18,000 and 24,000, the resistance between the two regions is essentially constant and the current increases linearly with voltage. Once this range is exceeded, the electrical field created under electrode 28,000 tends to effectively further pinch off the portion of semiconductor body 16,000 under region 20,000. This increases the resistance between regions 18,000 and 24,000 and thus limits current flow from one region to the other as voltage across the regions increases. Structure 10,000 thus acts as a resistor and as a current limiter.

Referring now to FIG. 3, there is illustrated a switching system 300 comprising control circuitry 310



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(within the largest dashed line rectangle) which is coupled by an output terminal 332 to the gate terminals of a pair of high voltage switching devices GDSL1 and GDSL2. The anode of GDSL1 and the cathode of GDSL2 are coupled to a first terminal Y0 and to a resistor R6 and the cathode of GDSL1 and the anode of GDSL2 are coupled to a second terminal X0 and to a resistor R5. This combination of GDSL1 and GDSL2 functions as a bidirectional switch which selectively couples terminals X0 and Y0 via a relatively low resistance path through GDSL1 or GDSL2. For illustrative purposes, these switches will be assumed to comprise the gated diode switch structure illustrated in FIG. 1. Control circuitry 310 functions so as to supply the needed potentials at terminal 332 and the current sourcing or sinking capability necessary to control the state of GDSL1 and GDSL2.

Control circuitry 310 essentially comprises a high voltage switch GDSC, a first voltage branch circuit 310A (illustrated within a dashed line rectangle) and a second voltage branch circuit 310B (illustrated with in another dashed line rectangle). Branch circuit 310A maintains the load switches GDSL1 and GDSL2 in an ON state such that conduction can occur through one or the other load switch if the potential of the anode and cathode terminals thereof is sufficient to support conduction or it can inhibit conduction through the load switches by maintaining the load switches in an OFF state. Branch circuit 310B serves to help switch GDSL1 and GDSL2 to an OFF state and therefore helps interrupt or inhibit conduction between X0 and Y0 independent of the potentials applied thereto so long as these applied potentials are within preselected limits.

Control circuitry 310 comprises a high voltage switch GDSC, which for illustrative purposes is the switch structure GDS2 illustrated in FIG. 1, a first current limiter CL1, which for illustrative purposes is the structure illustrated in FIG. 2, n-p-n transistors T1, T6,



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T7, and T8, p-n-p transistors T2, T3, T4, and T5, n-p-n phototransistors T9 and T10, which each have a photosensitive base region 341, 345, a diode D1, resistors R1, R2, R3, and R4, and a capacitor C1. A first  
5 input terminal 312 is coupled to R1, which is in turn coupled to the bases of T2 and T3 and to a terminal 314. The emitter of T2 is coupled to a terminal 316 and to R2, which is also coupled to a terminal 318, the emitter of T3 and the base of T4. The collector of T2 is coupled to the  
10 base of T1 and to a terminal 320. The collector and emitter of T1 are coupled to output terminal 332 and terminal X0, respectively. The collector of T3 is coupled to the collector of T6, the gate of GDSC, and to a terminal 322. The emitters of T4 and T5 are coupled  
15 together to a terminal 324 which is coupled to a first voltage supply (source) V1. The collector of T4 is coupled to the base of T5, one terminal of CL1, and to a terminal 326. A second terminal of CL1, in a preferred embodiment, is coupled to the cathode of GDSC and  
20 terminal 332, but it can instead be coupled to power supply (source) Vref as is indicated by the dashed line. The collector of T5 is coupled to the base of T6 and to a terminal 328. The emitter of T6 is coupled to the anode of GDSC, to the cathode of D1, and to a terminal 330. The  
25 cathode of GDSC is coupled to a second terminal of CL1 and to terminal 332. The anode of D1 is coupled to the emitter of T8 and to a terminal 338. The base of T8 is coupled to the emitter of T10 and to a terminal 340. The collectors of T8 and T10 are coupled together to the emitter of T7 and  
30 to a terminal 342. The base of T7 is coupled to a terminal 344 and to the emitter of T9. The collectors of T7 and T9 are coupled to one terminal of R4 and to a terminal 346. A second terminal of R4 is coupled to a first terminal of R3 and C1 and to a terminal 348. A  
35 second terminal of C1 is coupled to a terminal 352 which is coupled to a potential supply (source) Vref. A second terminal of R3 is coupled to a terminal 350 which is



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coupled to a potential supply (source) V2. The base regions of T9 and T10 are photosensitive. Terminal X0 is coupled through a resistor R5 to a terminal 354 which is coupled to a potential supply (source) V3. Terminal Y0 is  
5 coupled through a resistor R6 to a terminal 356 which is coupled to a potential supply (source) V4.

The combination of T7 and T9 form one photo-Darlington pair and the combination of T8 and T10 form a second Darlington pair. These two Darlington pairs are  
10 connected together in series. With light incident on the photosensitive base regions 341, 345 of T9 and T10, terminals 346 and 338 are coupled together via a relatively low impedance path. With the light removed, the two terminals are electrically isolated. The series  
15 combination of two such photo-Darlington pairs is used to provide a high voltage and high current capability switch. This allows control circuitry 310 to be electrically isolated from V2 by eliminating incident light on the bases of T9 and T10. Other high voltage and high current  
20 switches can be substituted for the photo-Darlington pairs.

The basic operation is as follows: Assuming X0 and Y0 are coupled through current limiting resistance (not illustrated) to +220 volts and -220 volts, respectively, conduction occurs through GDSL2 if the potential of gate  
25 terminal 332 is at a potential level which is near or below +220 volts. With V1 = +320 volts, V2 = +285 volts, Vref = 0 volts, and V3 = V4 = -48 volts, and current limiter CL1 limiting current therethrough to 1-  
14 microamperes, control circuitry 310 is capable of  
30 controlling the state of GDSL1 and GDSL2 by providing the needed potentials at terminal 332 and a source of current into terminal 332.

Assuming first that it is desired to set GDSL2 to an ON (conducting) state, an input voltage signal having a  
35 level of typically +315 volts (a low or "0") is applied to input terminal 312 and light is illuminated onto the photosensitive bases of T9 and T10. The emitter-base





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junctions of T2, T3, and T4 become forward-biased and the potential of the base of T1 (terminal 320) reaches a sufficiently positive potential with respect to the emitter (terminal X0) to forward-bias the emitter-base junction of T1 and thereby cause T1 to turn ON and pull down the potential of the collector thereof (terminal 332) to a value close to that of the potential of X0. This leaves the gate and anode of GDSL2 at close to the same potential and thus GDSL2 is in the ON state and conducts current from X0 to Y0. With T3 biased ON and conducting T4 is biased on since the emitter-base junction thereof is forward biased. Thus an electrical path through T4, CL1, T1 and R5 exists between V1 and V3. With T4 biased ON and conducting current through the emitter-collector thereof, the potential appearing at the base of T5 (terminal 326) is insufficient to forward-bias the emitter-base junction of T5 since the collector-emitter potential of T4 is designed to be less than the potential needed to forward-bias the emitter-base junction of T5. Thus, T5 is biased OFF and terminal 328 is electrically isolated from V1. Because the base terminal 328 of T6 is electrically floating, T6 is biased off. Terminals 328 and 330 are now electrically isolated from V1. The gate (terminal 322) of GDSC is at a potential near V1 since T3 is biased on. The anode terminal 330 is at a potential between approximately V1 and V2. While the anode terminal 330 is near V1 in potential, GDSC is ON and conducts until the potential of anode terminal 330 drops to approximately 20 volts below the potential of gate terminal 322. GDSC then switches OFF and conduction therethrough ceases. In addition, terminal 332 is also isolated from V2 since GDSC is OFF.

It is thus clear that branch circuit 310A serves to maintain load switch GDSL2 in the ON state and thus allows conduction therethrough.

Assume that it is now desired to switch GDSL2 to the OFF (blocking) state. Input terminal 312 is set to the level of +320 volts (a high level or "1"). This turns off



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T2, T3, and T4. T5 now becomes biased on and is typically operated in saturation such that terminal 328 rises in potential and forward-biases the emitter-base junction of T6. This brings the voltage of 330 near V1 and thus  
5 switches GDSC to the ON state. This causes terminal 332 to rise in potential to a level close to V1. This potential on terminal 332 is sufficient to switch GDSL2 to the OFF (blocking) state if there is a sufficient positive current flow into the gate of GDSL2. Minority carriers (e.g.,  
10 electrons) emitted at the cathode of GDSL2 and collected at the gate (terminal 332) constitute the equivalent of positive current flow from V1 through T5, the emitter-base junction of T6, GDSC, and into the gate of GDSL2. This current flow can be substantial and as a result it is  
15 necessary to have a high voltage and current device such as GDSC to switch GDSL2 to the OFF state. A high voltage and high current transistor would be expensive.

T5 is typically designed to have a relatively low current handling capability. As the current flow through  
20 T5 begins to increase, the voltage drop across the collector-emitter of T5 increases significantly until the potential of terminal 328 decreases to a level near V2. T5 then essentially limits further conduction therethrough. D1, which had previously been reverse-biased, now becomes  
25 forward-biased. With light incident on the photosensitive bases 345 and 341 of T9 and T10, respectively, positive current flows from C1 and V2 into terminal 330 and through GDSC and into the gate of GDSL2. The potential of terminal 330 drops to a level below but close to that of  
30 V2. The values of R3, R4, C1, and the potential of V2 are selected to provide substantially more current than can be provided by T5. Accordingly, GDSL2 is switched to the OFF state.

It is thus clear that 310A serves to essentially  
35 maintain GDSL2 in the OFF state and 310B serves to switch GDSL2 to the OFF state and to therefore help interrupt or inhibit conduction between X0 and Y0 independent of the



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potentials applied to X0 and Y0 so long as these applied potentials are within preselected limits.

If GDSL2 fails to switch OFF C1 becomes essentially discharged. Then the light incident on T9 and T10 is removed allowing C1 to recharge and terminal 312 is returned to +315 volts. This resets GDSC to the OFF state and allows GDSL2 to continue to be in the ON state and conducting. Light is again illuminated on the photosensitive bases of T9 and T10 and then the potential of 312 is raised back to +320 volts. GDSC is again switched to the ON state and another attempt is made at causing GDSL2 to be switched from the ON to the OFF state.

In one embodiment R1, R2, R3, R4, R5, and R6 are typically 1000,  $10^5$ ,  $10^4$ , 500,  $10^6$ , and  $10^6$  ohms, respectively, and C1 is 0.1 microfarads.

The combination of T7, T9, T8, and T10, which act as essentially a single high voltage and high current switch, are relatively expensive components. R3, R4, C1, T7, T9, T8, and T10 can be shared between a number of control circuitries 310.

If Y0 is more positive in potential than X0, then GDSL2 does not conduct and GDSL1 is affected in essentially the same manner as is described above for the operation of GDSL2.

Referring now to FIG. 4, there is illustrated a switching system 400 comprising control circuitry 410 (contained in the large dashed line rectangle), two pairs of bidirectional switches GDSL10, GDSL20, and GDSL3, GDSL4, and resistors R50, R60, R7, and R8.

Control circuitry 410 essentially comprises a first voltage branch 410A (illustrated within another dashed line rectangle) and a second voltage branch circuit 410B (illustrated within still another dashed line rectangle). The components of 410B are essentially the same as the components of 310B of FIG. 3, and they function in essentially the same way. The components of 410A are essentially the same as those of 310A of FIG. 1, except



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that four additional devices, n-p-n transistor T10A, p-n-p transistor T20A, and diodes D2 and D3 have been added to facilitate the controlling of a second bidirectional switch which comprises gated diode switches GDSL3 and GDSL4. An  
5 output terminal 438 of 410B is illustrated connected to the anodes of diodes D4, D5 . . . Dn. Each of these diodes represents a branch circuit which is essentially identical to 410A, and which has a separate pair of bidirectional switches, like GDSL10, GDSL20, and GDSL3 and GDSL4 coupled  
10 thereto. The control voltage branch 410B of control circuitry 400 is thus shared by n other control circuits which are essentially identical to 400.

D2 and D3 serve to electrically isolate terminals X00 and Y00 from X1 and Y1. T20A serves to control T10A in  
15 the same manner that T20 controls T10. Components of 400 which are essentially identical to components of control circuitry 310 of FIG. 3 have the same reference denotation with a "0" added thereto. Corresponding terminals have a "4" as the first reference number whereas in FIG. 3 the  
20 first reference number is a "3".

Control circuitry 400 has been built and found to be functional. Four voltage branch circuits 410A and one shared branch circuit 410B were used to control the states of eight pairs of gated diode switches. Each of the pairs  
25 of gated diode switches were similar to structure 10 of FIG. 1 except that there was no electrode coupled to region 40. Transistors T10 and T10A, and the corresponding six other transistors (not illustrated), were separate transistors. All of the circuitry of the first voltage  
30 branches 410A and the eight pairs of gated diode switches were fabricated on a single integrated circuit chip having an area of 14 square millimeters using dielectric isolation of components. The average turn-on time of a gated diode switch used with circuit 400 is 300 microseconds. The  
35 turn-off time is 50 microseconds. The average power dissipation of each of the branch circuits 410A is 5 milliwatts.



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The embodiments described herein are intended to be illustrative of the general principles of the present invention. Various modifications are possible consistent with the spirit of the invention. For example, transistor T6 of FIG. 3 and T60 of FIG. 4 can be eliminated. In such cases, the collector of T5 of FIG. 3 is connected directly to the anode of GDSC and the collector of T50 of FIG. 4 is connected directly to the anode of GDSC0. Still further, other high voltage and high current switches, such as a gated diode switch, could be substituted for the photo-Darlington pairs provided appropriate control circuitry is provided to control same. Still further, the junction transistors could be replaced by field effect transistors provided the polarities and magnitudes of the power supplies and circuit configurations are appropriately modified as is well known in the art. Still further, R1, R2, R3, R4, R5, and R6 can be standard integrated circuit resistors or pinch resistors. Still further, the current limiter can be a variety of different types of resistors or a junction field effect transistor. Still further, if at least one of the load GDSs of each pair is like GDS1 of FIG. 1, then the transistor which selectively causes the gate and cathode (anode) to be close to each other in potential, transistor T1 (T10A, T10...), is part of the GDS and terminal 320 (420, 420a...) is connected directly to electrode 50 (or its equivalent) of the load GDS. CL1 and CL10 can be connected to V2 and V20, respectively, instead of being connected to the cathodes of the respective GDSCs. D2 and D3 can be eliminated if a second control gated diode switch, like GDSC0, is added with its anode common to the anode of GDSC and its gate common to the gate of GDSC, and its cathode connected directly to the gates of GDSL3 and GDSL4. In this case the cathode of GDSC0 is connected directly to the gates of GDSL10 and GDSL20. Still further, T5 and T50 can be designed to have relatively high current capabilities. The load switches GDSLs can be switched to the OFF state solely by the first branch circuits 310A and



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410A so long as the current flow through the load switches GDSLs is within preselected limits. If this current flow is greater than these limits then the second branch circuits 310B and 410B are necessary to switch the load  
5 switches GDSLs to the OFF state.



Claims

1. Circuitry for use with a first switching device (GDSL1) of the type comprising a semiconductor body (16) a bulk portion of which is of a relatively high resistivity, a first region (18) of a relatively low resistivity type, a second region (24) of a relatively high resistivity type, a gate region (20) of a first conductivity type, a second conductivity type, the first and second regions being connected to output terminals of the switching device, the parameters of the second conductivity type, a gate region (20) being coupled to a control terminal of the switching device (GDSL1), the first (18), second (24) and gate (20) regions being mutually separated by portions of the semiconductor body bulk portion (16), the parameters of the device being such that, with a first voltage applied to the control terminal of the first switching device (GDSL1), a potential is established within a cross-sectional portion of the bulk of the semiconductor body (16) which is substantially different from that of the potential of the first (18) and second (24) regions and which prevents current flow between the first switching and second (24) regions, and that, with a second voltage applied to the control terminal of the first switching device (GDSL1) and with appropriate voltages applied to the output terminals (X0, Y0) of the first switching device, a relatively low resistance current path is established between the first (18) and second (24) regions by dual carrier injection,

CHARACTERIZED BY

circuit means (T1) having a control terminal and first and second output terminals;

the first output terminal of the circuit means being coupled to the control terminal of the switching device;

the second output terminal of the circuit means being coupled to one of the output terminals of the switching device;





21.

the control terminal of the circuit means being coupled to an input terminal of the circuitry; the circuit means being adapted to selectively cause the control device which is coupled to terminal of the switching device near to that of the output terminal of the circuit means.

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2. The circuitry of claim 1 CHARACTERIZED BY a second switching device (GDSC); an output terminal (332) of the second switching device coupled to the control terminal of the first switching device;

15

3. The circuitry of claim 2 further CHARACTERIZED IN THAT the second switching device is of the same type as the first switching device (GDSC);

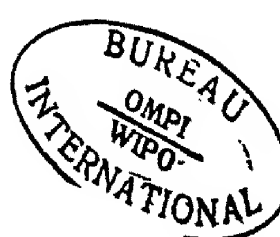
20

a second branch circuit (310B) is coupled to the first switching device (GDSC); the first branch circuit (310A) is adapted to be coupled to a first potential source (V1); and the second switching device (GDSC) is adapted to be coupled to a second potential source (V2) which is adapted to supply current into the first output terminal of the second switching device (GDSC) if said output terminal assumes a preselected potential level.

30

4. The circuitry of claim 3 further CHARACTERIZED IN THAT the first branch circuit (310A) comprises a third switching device (T5) having output circuitry (328) coupled to the first output terminal (330) of the second switching device (GDSC) and having a control terminal (312) of the circuitry, the third switching device (T5) being adapted to selectively electrically isolate the first output terminal (330) of the second switching device (GDSC) from the first

35



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potential source (V1); and

the second branch circuit (310B) comprises a fourth switching device (T7, T8, T9, T10) having output circuitry (338) coupled to the first output terminal (330) of the second switching device (GDSC) and having a control portion (341, 345), the fourth switching device (T7, T8, T9, T10) being adapted to selectively electrically isolate the first output terminal (330) of the second switching device (GDSC) from the second potential source (V2).

5. The circuitry of claim 4 further  
CHARACTERIZED BY

a first resistor (CL1) which is coupled to the control terminal (326) of the third switching device (T5).

6. The circuitry of claim 5 further  
CHARACTERIZED IN THAT

the resistor is a current limiter (CL1) and that it is also coupled to the second output terminal (332) of the second switching device (GDSC).

7. The circuitry of claim 6 further  
CHARACTERIZED BY

a fifth switching device (T3) which has output circuitry (318) adapted to be coupled to the first potential source (V1) and to the control terminal (322) of the second switching device (GDSC), the fifth switching device (T3) having a control terminal (314) coupled to the input terminal (312) of the circuitry.

8. The circuitry of claim 7 further

CHARACTERIZED IN THAT

the first branch circuit (310A) comprises a diode (D1) whose cathode is coupled to the first output terminal (330) of the second switching device (GDSC) and whose anode is coupled to an output terminal (338) of the fourth switching device (T7, T8, T9, T10);

sixth (T2), seventh (T4), and eighth (T6) switching devices each have a control terminal and output



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circuitry;

the control terminal (314) of the sixth switching device (T2) is coupled to the circuitry input terminal (312) and the output circuitry is coupled to the output circuitry (318) of the fifth switching device (T3), the control terminal of the seventh switching device (T4), and to the control terminal (320) of the circuit means (T1),

there is further included a capacitor (C1), a second (R1), third (R2), fourth (R3), and fifth (R4) resistors;

the second resistor (R1) is coupled to the circuitry input terminal (312) and to the control terminal (314) of the sixth switching device (T2);

the third resistor (R2) is coupled to the output circuitry (316) of the sixth switching device (T2) and to the output circuitry (318) of the fifth switching device (T3);

the fifth resistor (R4) is coupled to an output terminal (346) of the fourth switching device (T7, T8, T9, T10) and to a first terminal (348) of the capacitor (C1) and to the fourth resistor (R3); and

the fourth resistor (R3) is adapted to be coupled to the second potential source (V2).

9. The circuitry of claim 8

CHARACTERIZED BY

sixth (R5) and seventh (R6) resistors;

the sixth (R5) resistor being coupled to one of the output terminals (X0) of the first switching device (GDSDL1) and the seventh (R6) resistor being coupled to the other output terminal (Y0);

an eighth switching device (T6) which is an n-p-n transistor with the collector (322) coupled to the output circuitry of the fifth switching device (T3); the base coupled to the output circuitry (328) of the third switching device (T5), and the emitter coupled to the first output terminal (330) of the second switching device (GDSC).



24.

10. The circuitry of claim 9

CHARACTERIZED BY

the first (GDSL1) and second (GDSC) switching devices being gated diode switches.

11. The circuitry of claim 1

CHARACTERIZED BY

the circuit means (T1) being an integral part of the first switching device (GDSL1); and

the first switching device (GDSL1) having a shield (base) region (22, 40, 46) which surrounds the second region (24), said shield (base) region (22, 40, 46) being of the first conductivity type and having a separate control terminal (50) connected thereto.



FIG. 1

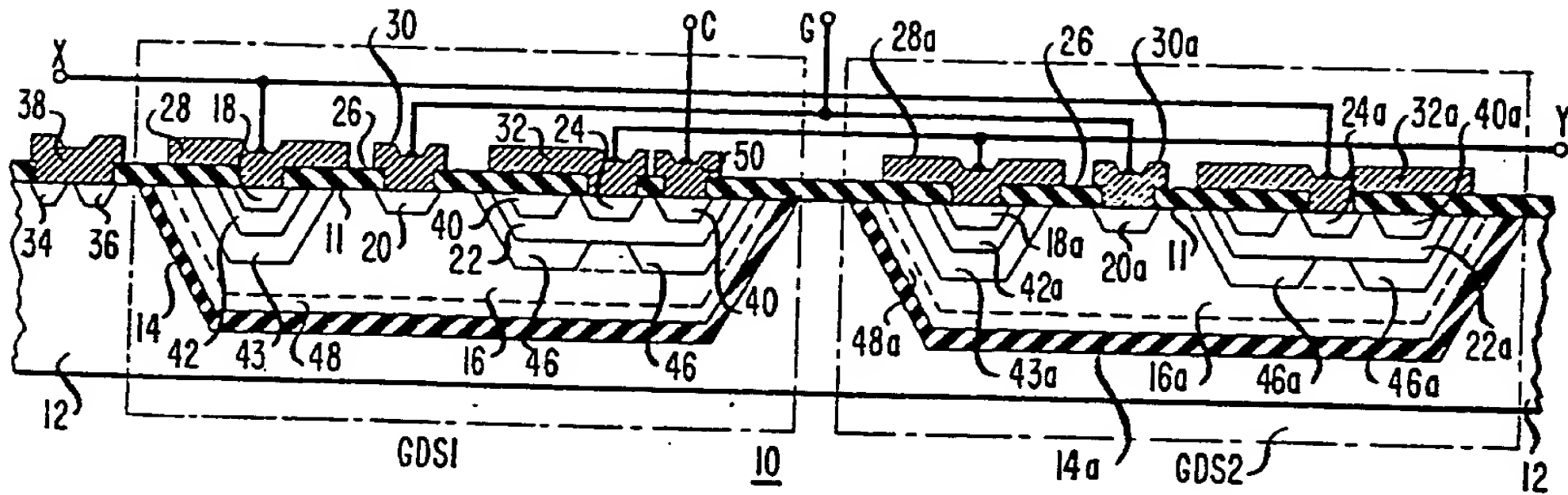


FIG. 2

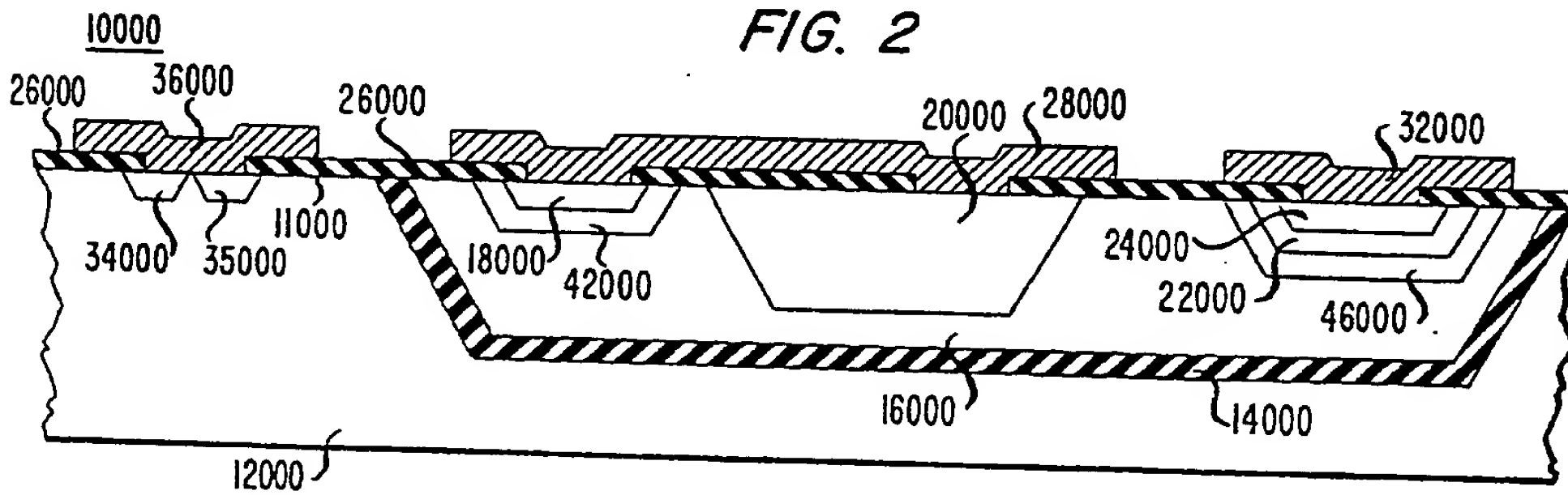
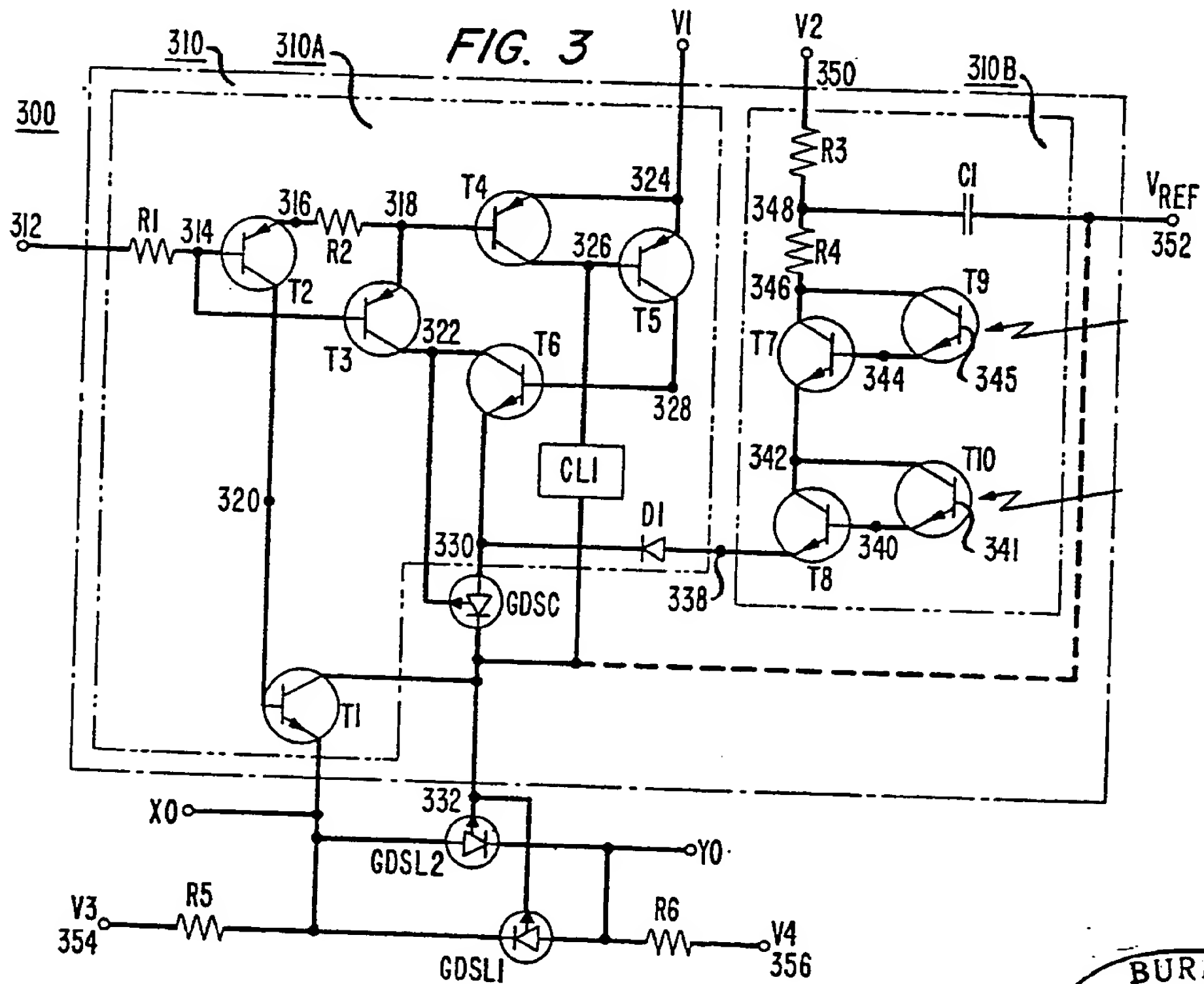
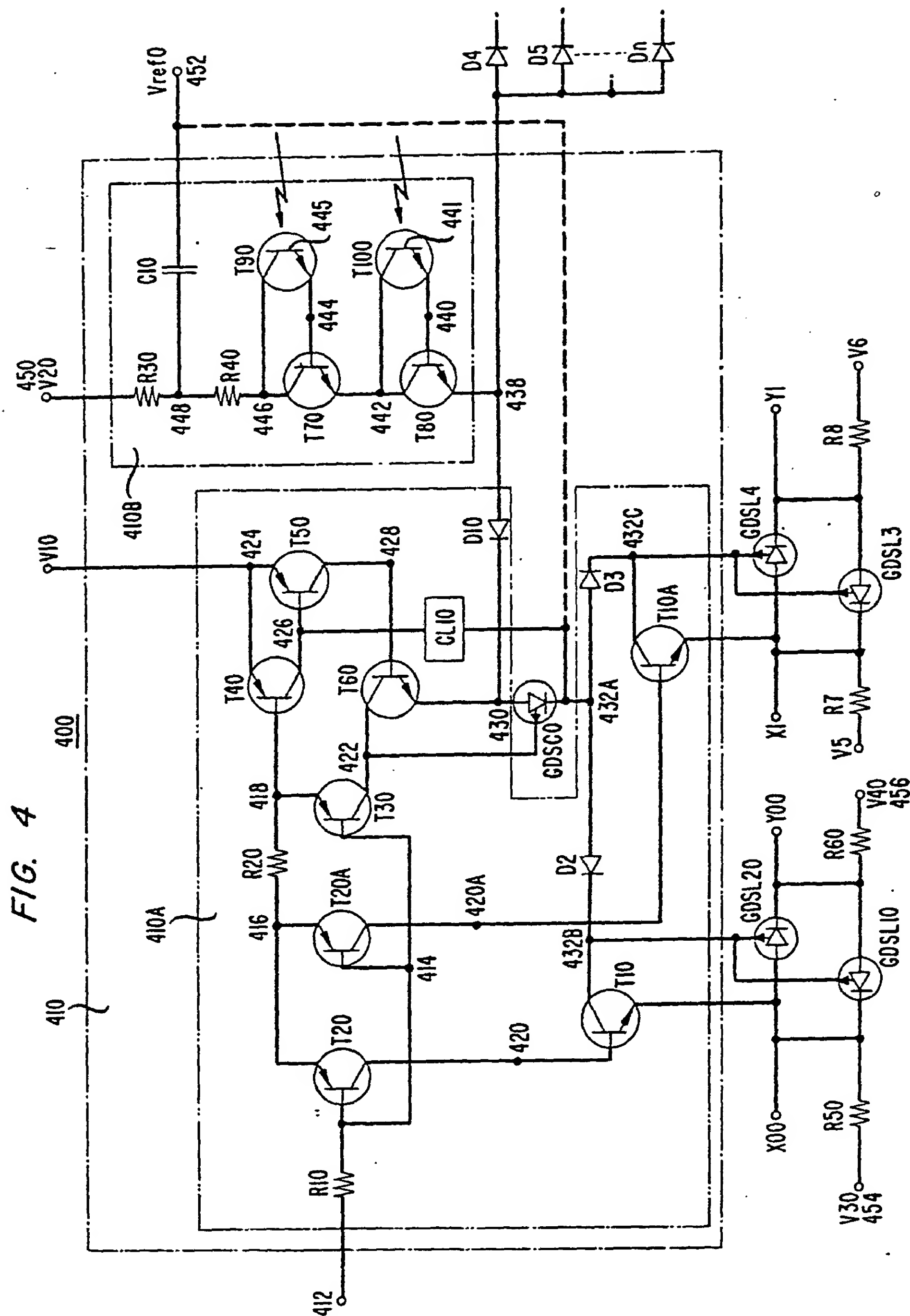


FIG. 3





# INTERNATIONAL SEARCH REPORT

International Application No PCT/US80/01696

<b>I. CLASSIFICATION OF SUBJECT MATTER</b> (If several classification symbols apply, indicate all) <sup>3</sup>		
According to International Patent Classification (IPC) or to both National Classification and IPC		
INT. CL. <sup>3</sup> H03K 17/60, 3/35, 3/353; H01L 29/80, 29/74, 29/12		
U.S. CL. 307/252A, 252C, 252J, 252K, 304, 305; 357/22, 38, 58		
<b>II. FIELDS SEARCHED</b>		
Minimum Documentation Searched <sup>4</sup>		
Classification System	Classification Symbols	
U.S.	307/252A, 252C, 252J, 252K, 304, 305 357/22, 38, 58	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched <sup>5</sup>		
<b>III. DOCUMENTS CONSIDERED TO BE RELEVANT</b> <sup>14</sup>		
Category <sup>9</sup>	Citation of Document, <sup>15</sup> with indication, where appropriate, of the relevant passages <sup>17</sup>	Relevant to Claim No. <sup>18</sup>
X	US, A, 3,891,866, PUBLISHED 24 JUNE 1975, OKUHARA ET AL.	1-11
A	US, A, 4,060,821, PUBLISHED 29 NOVEMBER 1977, HOUSTON ET AL.	1-11
X	US, A, 4,117,350, PUBLISHED 26 SEPTEMBER 1978, KALFUS ET AL.	3-10
A	US, A, 4,132,996, PUBLISHED 02 JANUARY 1979, BALIGA	1-11
X,P	US, A, 4,224,634, PUBLISHED 23 SEPTEMBER 1980, SVEDBERG	1-11
A,T	US, A, 4,242,697, PUBLISHED 30 DECEMBER 1980, BERTHOLD ET AL.	1-11
<p><sup>16</sup> Special categories of cited documents:</p> <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>"A" document defining the general state of the art</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document cited for special reason other than those referred to in the other categories</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> </div> <div style="width: 45%;"> <p>"P" document published prior to the international filing date but on or after the priority date claimed</p> <p>"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance</p> </div> </div>		
<b>IV. CERTIFICATION</b>		
Date of the Actual Completion of the International Search <sup>2</sup>		Date of Mailing of this International Search Report <sup>2</sup>
02 APRIL 1981		16 APR 1981
International Searching Authority <sup>1</sup>		Signature of Authorized Officer <sup>20</sup>
ISA/US		JOSEPH E. CLAWSON, JR.